In the claims:

1. A method of conserving power in a WLAN receiver comprising the steps of:

enabling a channel estimator only during the preamble of each packet and storing and using said channel estimator values for the duration of the packet.

2. A method of conserving power in a WLAN receiver comprising the steps of:

enabling a channel estimator only during the preamble of each packet and running pilot processing after the preamble of each packet to get off set error values from the channel estimation pilot processing values.

3. The method of claim 2 including the step of storing and using said channel estimator values for the duration of the packet.

4. The method of claim 3 including the step of summing said stored channel estimator values for the duration of the packet with said off set error values determined by the pilot processing.

5. A system for conserving power in a WLAN receiver comprising:

an equalizer;

a channel estimator for detecting transmitted errors in a transmitted packet and providing equalization to said equalizer for the detected channel errors; and

means response to the start of each packet for enabling said channel estimator during the preamble and thereafter disabling said channel estimator for the remainder of the packet and storing the estimated value for the duration of the packet.

6. The system of claim 5 including a separate pilot processor for detecting off set errors from the channel estimation and providing off set correction to said equalizer for the whole data portion of the packet after the preamble.

7. The system of claim 6 wherein said stored channel estimator values for the duration of the packet is summed with said off set error values determined by the pilot processing.

8. The system of claim 7 wherein said equalizer includes a frequency domain equalizer.

9. The system of claim 7 wherein said equalizer includes a time domain equalizer.

10. The system of claim 7 wherein said equalizer is a frequency domain equalizer and a time domain equalizer.

11. The system of claim 6 wherein said equalizer is a frequency domain equalizer and a time domain equalizer.

12. The system of claim 5 wherein said means for enabling and disabling said channel estimator includes a means for decoding the status of the receiver state machine.

13, The system of claim 6 wherein said means for enabling and disabling said channel estimator and enabling said separate pilot processing equalizer for the whole data portion of the packet after the preamble includes a means for decoding the status of the receiver state machine.